and drawings. No new matter has been added to the application by these amendments.

The objection to the drawings is duly noted. The Examiner states that a "first circuit" a "second circuit" and a "control circuit", as set forth in claims 14 and 16 must be shown or the features must be canceled from the claims and no new matter should be entered.

Although the Examiner states that a proposed drawing correction or corrected drawings are required in reply to the Office Action to avoid abandonment of the application, Applicants submit that no drawing is required. It is submitted that claim 14 reads, for example, on Figure 3 as follows:

An input signal is applied to input pad P having a parasitic capacitance Cp; a first circuit element 56 selectively provides current to the parasitic capacitance. A second circuit element 58 selectively prevents discharge of the parasitic capacitance and a control circuit comprised of elements 40 through 54 turns on the first circuit element 56 and turns off the second circuit element 58 when a positive going edge of the input is detected and turns off the first circuit element 56 and turns on the second circuit element 58 when a negative going edge of the input signal is detected.

Regarding claim 16, the first and second elements, 56 and 58, are transistors. It is therefore submitted that these claims read on an existing figure of the application and no new figure is needed since Figure 3 shows all the features recited in claims 14 and 16. It is

therefore submitted that the objection to the drawing should be withdrawn.

The objection to claims 2 and 11 is duly noted. The amendments proposed by the Examiner have been adopted and incorporated into these claims and it is submitted that this objection should therefore be withdrawn.

Claims 14-17 and 24 have been rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

Regarding claim 14, as is pointed out hereinabove, this claim clearly reads on Figure 3 and the "first circuit 56 and the second circuit 58 both have control inputs to selectively either provide current or prevent discharge to (from) the parasitic capacitance. Regarding the phrase "into said input", this phrase has been omitted from claim 14 to cure this informality. It is submitted that the above arguments hold with equal measure with regard to claim 16 and, for the above reasons, it is submitted that the rejection of claims 14-17 and 24 should be withdrawn.

Claims 1-6, 8, 9, 11-15 and 18-27 have been rejected under 35 U.S.C. §102(e) as anticipated by Ishikawa et al. (JP Patent '430). This rejection is respectfully traversed.

Firstly it should be noted that JP '430 does **not** constitute prior art since its publication date is September 14, 2000. The present application was granted a filing date in the United States Patent and Trademark Office of August 31, 2000 which clearly predates the

publication date of JP '430 and for these reasons it is submitted that this rejection should be withdrawn.

In addition to the above, with respect to 1 and 2, the Action states that Figure 1 of Ishikawa shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance. However, Ishikawa, Figure 1 is not an input/output device. An input/output device is supposed to have only one pin (pad P) that might transmit signals in a transmission mode in which case it acts as an output device, or receive incoming input signal in receiving mode (when transmitter is disabled) to be an input device. In Figure 1, Ishikawa shows two separate pins. One is an input and the second is an output. Based on Ishikawa, Figure 1, this circuit would in fact be characterized as an input amplifier, or an input level shifter, or an input buffer, but it is not an input/output device.

It is noted that disabled transmitters usually have pretty big parasitic capacitor between input/output pin (pad P) and ground. There nothing of this kind in input or input/output devices having only two serially connected parasitic

capacitors with middle point access. Even if JFET transistor that Ishikawa is using consists of two serial connected parasitic capacitors with their middle point access (Ishikawa Fig.4) it is absolutely clear from the same Ishikawa Fig.4 that there is another parasitic capacitor between the input and ground. As shown in Ishikawa Fig.4. There are two serial connected parasitic capacitors (gate 103 and diffusion area 102), and (diffusion area 102 and grounded p-p+ substrate 101), and there is also an overlapping parasitic capacitor between the gate 103 and the p+ substrate 101 (GND). There is no question that there is an additional parasitic capacitor between input and ground in Ishikawa Fig.4 JFET transistor structure.

In addition, the statement at page 6, lines 1-4 of the Action that "... The parasitic capacitor Cp is the combination of the capacitances formed by the gate and the source or by gate and the drain....combined with the capacitance formed by PAD, the connecting wire and the substrate" is clearly incorrect. In Ishikawa there is another single equivalent parasitic capacitor between the input and the ground. There is also no clear indication that all of these additional parasitic capacitors are really serial connected capacitors with the access to their middle

point.

Ishikawa Fig.1 shows two serial connected parasitic capacitors with access to their middle point (JFET gate-to-channel, and channel to p-p+ substrate capacitors), as well as parasitic capacitor between input and ground (Ishikawa Fig.4 gate to p-p+ substrate overlapped capacitor) as well as parasitic capacitor between input and ground (Ishikawa Fig.1 buffer 6 input capacitor), as well as parasitic capacitors between input and ground that related to package, pad and substrate (the examiner report page 6, line 1-4).

As soon as there is at least one additional parasitic capacitor between input and ground in addition to two serial connected parasitic capacitors with middle point access, the input signal will have to charge or discharge these parasitic capacitors. That means the incoming input signal will be damaged. <u>This is exactly the opposite of the present invention.</u> The claims are all directed to a method or apparatus for reducing distortion by introducing a current to the parasitic capacitance to compensate for current that would have been drained from the signal. Accordingly, it is respectfully submitted that the pending claims would be

patentable over Ishikawa.

Additionally, the Action erroneously states that Ishikawa Fig.1 "introduce[es] current to the parasitic capacitor 3 via buffer 6 at the positive edge of the input signal ..." (page 3, lines 21-22). However, this cannot be correct because Ishikawa Fig.1 does not introduce any current to the parasitic capacitor 3.

The Action also erroneously states that "... the parasitic capacitance (4) is across the input (1) and ground" (page3, line 28). However, according to Ishikawa Fig.1, Ishikawa Fig.2, and Ishikawa Fig.3 the parasitic capacitance (4) is connected between the ground and parasitic capacitance (3). It is not connected across the input (1) and ground.

There is no suggestion in Ishikawa of the present invention. As shown in Ishikawa Fig.4, there is another single parasitic capacitor between input and ground (as a combination of many factors noted by the Examiner in the Action). Because of this additional parasitic capacitor, the incoming input signal will be damaged.

If the Examiner believes that any additional formal matters need to be

addressed in order to place the present application in condition for allowance, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendments and Remarks, it is respectfully submitted that the present application, including claims 1-6 and 11-27, is in condition for allowance, and a notice to that effect is respectfully requested.

Respectfully submitted,

Drapkin et al.

Reg No. 34,626

By for Louis Weinstein

Louis Weinstein
Registration No. 20,477
(215) 568-6400

Volpe and Koenig, P.C.
Suite 400, One Penn Center
1617 John F. Kennedy Boulevard
Philadelphia, PA 19103

LW/RJH/ns

MARKED-UP SPECIFICATION AND CLAIMS UNDER 37 CFR 1.121

IN THE SPECIFICATION

Page 4, beginning at line 11:

At high operating frequencies, it cannot be assumed that the input of the receiver R is an open circuit into the presence of an input parasitic capacitor in order to be able to treat the receiver R as an open circuit, thus the signal applied to the input of the receiver R [is to] will charge/discharge the parasitic capacitor. Such charging/discharging means that the signal that is received by the receiver R will be distorted. The same situation occurs with the parallel termination shown in Figure 1B wherein a terminating resistor R_{TERM} is in parallel with the parasitic capacitance Cp. In addition, the higher the frequency, the greater the distortion. This distortion is particularly referred to as a "glitch" when the receiver has to have a strong signal and a spike is heard as a result of the distortion.

Page 5, beginning at line 28:

In operation, during a rising edge signal (+dv/dt), since the voltage of C_T cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the drain of PMOS transistor 20 to provide sufficient current at terminal 24 to compensate for a portion of the input current that would otherwise be provided to parasitic capacitance [C_T] Cp by the input signal.

IN THE CLAIMS

2. (TWICE AMENDED) The method of claim 1, wherein said signal is applied to an input of [an] said circuit.

11. (AMENDED) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capcitance, comprising [the steps of]:

a detecting circuit for detecting a change in voltage of said input signal; and

a correction circuit for changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

14. (Amended) Apparatus for reducing distortion of [a] an input signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance at said input, compromising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capacitance [into said input]; and

a control circuit monitoring said input signal for respectively turning on said first

circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of said input signal is detected.

16. (TWICE AMENDED) Apparatus for reducing distortion of [a] an input signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance at said input, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capcitance [into said input]; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of second circuit element when a negative going edge of said input signal is detected;

said first and second circuit elements have a common terminal coupled to said parasitic capacitance;

said first and second circuit elements being transistors.